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Monolithic integration of superconducting-nanowire single-photon detectors with Josephson junctions for scalable single-photon sensing

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Abstract

We demonstrate superconducting single-photon detectors (SPDs) that integrate signals locally at each pixel. This capability is realized by the monolithic integration of superconducting-nanowire SPDs with Josephson electronics. The motivation is to realize superconducting sensor elements with integrating capabilities similar to their CMOS-sensor counterparts. The pixels can operate in several modes. First, we demonstrate that photons can be counted individually, with each detection event adding an identical amount of supercurrent to an integrating element. Second, we demonstrate an active gain control option, in which the signal added per detection event can be dynamically adjusted to account for variable light conditions. Additionally, the pixels can either retain signal indefinitely to record all counts incurred over an integration period, or the pixels can record a fading signal of detection events within a decay time constant. We describe additional semiconductor readout circuitry that will be used in future work to realize scalable, large-format sensor arrays of superconducting SPDs compatible with CMOS array readout architectures.

Keywords: superconducting electronics, Single photon detectors, monolithic integration

1. Introduction

Superconducting-nanowire single-photon detectors (SPDs) are gaining maturity with reported system detection efficiencies greater than 98% [1] and timing jitter below 3 ps [2]. These devices can detect single quanta of radiation, and the same basic device concept can be used from the UV to mid-IR [3], with recent demonstrations showing high efficiency up to 10 μm wavelength [3]. SPDs have very low dark counts and can be fabricated with a simple process into relatively large (400 kilopixel) arrays [4]. Large arrays are desirable for many purposes such as imaging and spectroscopy with applications including astronomy [5], semiconductor circuit metrology [6, 7], and biomedical imaging [8, 9]. However, readout of large arrays remains the primary impediment to adoption in deployed systems. When an SPD detects a photon, the bias current is diverted from the wire. Room temperature amplifiers and digital electronics are typically used to read out the current pulses from each detector independently. This

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approach often requires large numbers of coaxial cables inside the cryostat and extensive room-temperature electronics, limiting scaling to larger arrays. Additionally, when detecting photons deeper in the mid-IR, the energy of the photons decreases, necessitating narrower nanowires, which carry less current and provide smaller pulses for detection. Directly amplifying and measuring each diverted current pulse is not an ideal measurement technique for large arrays of SPDs. For the largest arrays demonstrated to date [4], multiplexed readout lines are employed that limit total system count rates, and the means of encoding SPD detection events onto the readout line requires large SPD currents, which makes operation with mid-infrared SPDs difficult.

Several approaches to readout of SPDs [10] involve the transduction of pulses from the SPD to supercurrent using superconducting electronic circuitry. Example approaches include using circuitry based on nanowires [11] or Josephson junctions (JJs). When using JJs, it is possible to leverage superconducting quantum interference devices (SQUIDs) as sensitive flux-to-voltage transducers [12] or to make use of digital processing with single-flux-quantum circuits [13–16] or adiabatic quantum flux parametron circuits [17–20]. Most of these efforts using JJs to readout SPDs have employed separate chips for the sensors and the readout electronics with wire bonds between the specialized die; two recent demonstrations have accomplished monolithic integration of SPDs with JJs [21, 22].

Here we propose and demonstrate an approach to large-scale SPD array readout that makes use of SPDs integrated with JJs and SQUIDs to introduce a technique of photon count integration akin to CMOS cameras. We demonstrate single-photon integrating pixels suitable for this approach wherein the history of photon detection events is locally stored at each pixel, analogous to charge accumulation in CMOS sensors [23]. Circuits performing the desired functions can be achieved through the monolithic integration of SPDs with JJs. In these circuits, an SPD works in conjunction with JJ circuits to transduce photon detection events into current that can be stored indefinitely in a superconducting loop at each pixel. This approach decouples detection events from the readout process. Low-noise readout can be accomplished through a measurement duration that is not limited by the temporal extent of the SPD current pulse. This measurement can be accomplished with MOSFET circuits that transduce the integrated current signal to charge on a capacitor. At that point, the readout proceeds exactly as in a CMOS sensor array. SPD-JJ integration circumvents the small SPD current signal in the mid-IR regime, as explained later. Further integration with MOSFETs enables a low-noise, scalable readout framework that never misses an SPD count, only sends the required information to room temperature, and transduces low-voltage superconductor signals to semiconductor-level voltages to be processed by conventional silicon electronics. This integrated approach leverages the best attributes of superconducting sensors with the convenience and fieldability of semiconductor array readout concepts. While monolithic integration appears feasible and should be pursued, the superconducting circuits could also be bump bonded to CMOS readout circuits, which would allow the complete circuits to be fabricated with existing processes. In this work we demonstrate the first processing stage of this concept where the SPD signal is transduced to integrated supercurrent by JJ circuits. The further integration with MOSFETs will be the subject of future work.

2. Photon counter circuit

The single-photon integrating pixel concept demonstrated here is shown in figure 1. A detection event from the SPD is converted into a single-flux quantum (SFQ) through an inductively-coupled DC-SFQ converter [24, 25]. The SFQ pulse leaving the DC-SFQ converter then propagates down a short Josephson transmission line and is added to an integration loop at the pixel. The Josephson transmission line comprises two junctions between the DC-SFQ converter and the integration loop, as shown in figure 1(a). One benefit of this approach is that the input to the DC-SFQ converter is not current, but rather magnetic flux, which is the product of current and mutual inductance. The mutual inductance between the SPD and the DC-SFQ converter can be quite large, limited primarily by space, enabling even small SPD pulses to generate SFQ pulses. SPD output currents can be as small as 1 μA when detecting long-wavelength photons in the mid-IR. The price is area, with the DC-SFQ converter receiving the SPD pulse requiring an area of 30 μm $\times$ 30 μm. Still, a megapixel array would fit on a 3 cm $\times$ 3 cm sensor chip. Therefore, by integrating JJs with SPDs we can overcome the limitation of small current signals and provide local integration of the signal at each pixel. Timing information is retained at the level of a 10 kHz frame rate (100 μs) as opposed to the sub-ns jitter of the detection event. The retained temporal information is more than sufficient for imaging and some spectroscopic applications. By separating photon detection and integrated signal measurement, we can integrate photon counts for as long as desired and separately measure the accumulated signal for as long as necessary to realize noiseless readout.

The circuit in figure 1(a) involves an SPD, a DC-SFQ converter (topologically equivalent to a DC SQUID), a Josephson transmission line, an integration loop that stores the pulses, and a readout component. A readout SQUID is used in this report as the readout component, but in the final scheme a row-column bus architecture identical to CMOS sensor arrays is envisioned, as discussed in section 5. The first step in the circuit operation is the detection of a photon by the SPD. When a photon that is absorbed by the SPD breaks superconductivity and causes a resistive hot spot [26], the bias current I_{b0} will be diverted from the SPD into a transformer coupled to the SPD-to-SFQ SQUID, labelled as SFQ in figure 1(a). Simulation of the SPD current pulses, I_{spd}, are shown in figure 1(b) by the blue curve. The next step is the transduction of each detected photon into an individual fluxon. A fluxon is a quantum of magnetic flux denoted by and equal to $\Phi_0 \equiv h/2e \approx 2\,\text{mV}\cdot$ ps. Each fluxon generated by the SPD-SFQ transducer circuit propagates through a Josephson transmission line and is

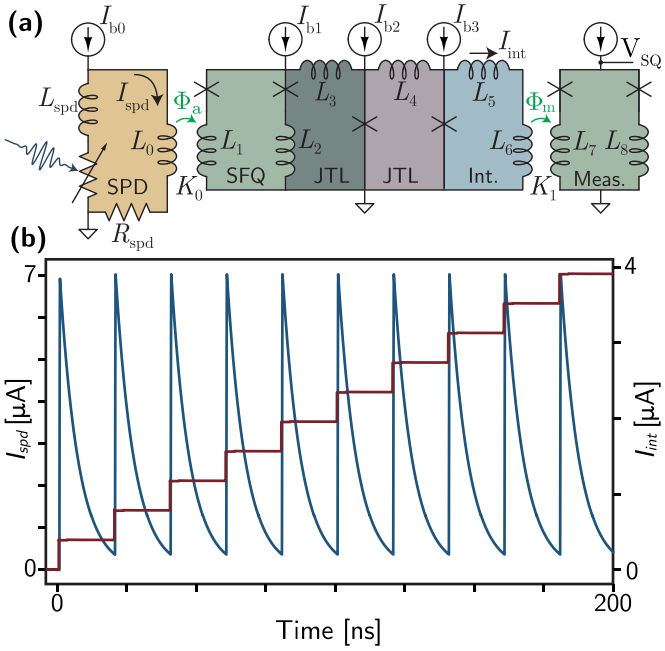

Figure 1. (a) Schematic of superconducting single photon counter. Parameters used in simulation and design are the same, except R_{spd} which was increased from 12.375 Ω to 123.75 Ω in simulation, to reduce simulation time. The rest of the parameters were $L_{spd} = 825$ nH, $L_0 = 3.1$ nH, $L_1 = 12.7$ pH, $L_2 = 1.1$ pH, $L_3 = L_4 = 10.34$ pH, $L_5 = 5.3$ nH, $L_6 = 0.18$ nH, $L_7 = 9.36$ pH, $L_8 = 0.8$ pH. Mutual inductance couplings were $K_0 = 0.5$ and $K_1 = 0.25$. The critical current (I_c) of all Josephson junctions was 100 μA. The simulation bias currents were $I_{b0} = 10\,\mu A$, $I_{b1} = 140\,\mu A$, $I_{b2} = I_{b3} = 70\,\mu A$. (b) Circuit simulation. The blue curve is the current diverted from the SPD (I_{spd}), which is plotted relative to the left y-axis. The red curve is the current being integrated in response to each SPD pulse (I_{int}), which is plotted relative to the right y-axis.

stored as current in an integration loop. In the present case, the SPD provides flux input after each photon detection event, producing a discrete amount of supercurrent that is stored in an inductive loop after passing through the Josephson transmission line, which we refer to as the detector integration (DI) loop. In response to a single photon detection event, the integrated current can either be in the form of a single flux quantum or it can be in the form of several flux-quantum pulses. In the former case we have digital operation with each photon detection event producing an identical current signal, which we refer to as SPD-SFQ operation or the digital mode. In this case, the amount of current added to the loop per photon detection is Φ_0/L, where L is the loop inductance. Current in the integration loop is shown by the red curve in figure 1(b). In the latter case each photon leads to an analog signal that can be adjusted with a control bias (I_{b1}). The main advantage of the digital mode of operation is that it is conducive to zero-noise operation and less dependent on circuit bias current, I_{b1}. There is a one-to-one correspondence between the number of detected photons and stored fluxons. This results in a near-perfectly linear relationship between photon count and integrated signal. The amplitude of added signal accumulated with each photon detection event is identical across an extremely broad range. With this mode of operation, 1024 photon pulses can be detected with exactly linear response across all pulses. On the other hand, the advantage of the analog mode is that the amplitude of the signal can be adapted by adjusting the bias current, I_{b1}, which enables gain control for adjustable performance depending on the light level. The same hardware infrastructure supports both modes of operation.

In either the analog or digital case, the generated current is stored in the integration loop where the signals from repeated photon-detection events are summed. With the integration loop there are again two modes of operation. In one mode the loop has zero resistance, and the signal is stored with no decay, as shown in figure 1(b). In this mode of operation, the current stored in the loop immediately preceding a read event is proportional to the total number of photons that have been detected in that integrate-read cycle. In the second mode, the integration loop has a finite resistance, and the integrated signal leaks with a rate given by the loop $\tau = L/r$ time constant [21]. The signal stored in the pixel is proportional to the rate of photon detection events in the preceding time interval of order τ. In this mode of operation, no external signal is required to reset the state of the loop. This is a leaky integrator wherein the signal is proportional to the recent rate of photon detection events, so in this mode the sensor is a power meter (assuming incident photons of uniform energy). The exact same pixel can be used in either power or energy integration mode with the inclusion of a simple resistive element. In this work we demonstrate single pixels, but the readout concept is intended to scale to large arrays.

For other applications that require precise timing information, similar circuits can be used. With minor modifications, each pixel can be engineered to store a current proportional to the time of arrival of a photon relative to a clock. This approach leverages the high switching speed of JJs to potentially store timing information with picosecond resolution. Readout proceeds identically to the case of the photon-counting pixels presented here. Exploration of these timing pixels will be the subject of future work.

3. Fabrication

The fabrication consists of fifteen mask layers. Electron-beam lithography was used for the SPD step, while all other patterning was accomplished with photolithography using a 365 nm *i*-line stepper. A complete process flow can be found in [21]. In brief, a 40 nm Nb wiring layer for contact to the SPDs was patterned using a liftoff process. Liftoff was used to avoid a vertical edge and provide a gradual, sloping contact for the thin film used for the SPDs. The SPDs were formed from a 4.1 nm thick MoSi film [27], which was sputtered after the Nb contact layer. The MoSi was patterned into a detector meander using electron-beam lithography to realize wire widths around 200 nm. An interlayer dielectric of SiO_2 insulates the SPD layer from a Nb ground plane above it. The JJ trilayer stack (Nb-aSi-Nb) [28] is then deposited and patterned above the

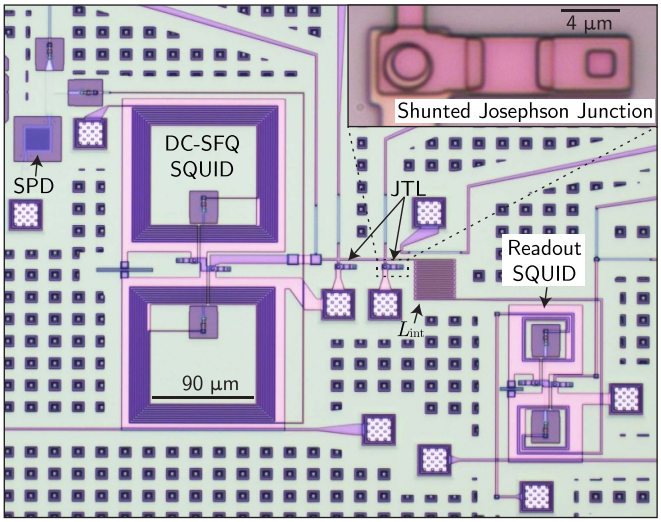

Figure 2. Microscope image of the fabricated device.

ground plane, with another SiO_2 insulator in between. PdAu resistors are patterned and deposited with liftoff to form the JJ shunt resistors. An additional low-resistance Au layer was used to make resistors with small values and therefore long attainable leak time constants in the integrating loops used in power-meter mode, described in section 4. An additional top insulator sealed the structures. All layers were connected with Nb vias through the insulators. Microscope images of the fabricated device are shown in figure 2.

Roughly 12 devices from this wafer were tested, and all operated close to designed performance. There were no failures due to fabrication issues. The JJ cross-wafer I_c variation was around $\pm 20\%$ from the center to the edge of the 76.2 mm wafer, with the nominal value residing in a ring of half the wafer radius. Such variation is typical for this process and this sputtering tool.

A major challenge for this SPD readout concept is to reduce the size of the readout circuitry while achieving a high SPD fill factor. Two fabrication improvements will enable circuit size reduction. First, lithography with higher resolution for the wiring layers would enable reduction of the size of the input coil into the transduction SQUID by at least a factor of 100 by reducing the wire width from 1 μm to 200 nm and wire thickness from 200 nm to 20 nm. Second, by utilizing a damascene process with planarization between each layer, the components of the circuit can be stacked vertically. This would significantly reduce the overall footprint of the circuit and enable the SPD meander to be on the top layer, spread above the transduction and readout circuitry below. Such a fabrication process would be the default for a mature foundry, but the unplanarized process is much more tractable in NIST's research cleanroom.

4. Experimental characterization

Measurements were performed at 2.3 K in a closed-cycle Gifford–McMahon cryostat. The chip was flood illuminated by a fiber-coupled, 780 nm pulsed laser source. The availability of an inexpensive, pulsed laser source was the only reason this wavelength was used. The circuit concept should be applicable for SPDs from the UV to the mid-IR. The laser pulse width was approximately 480 ps, while the SPD recovery time was around 37.5 ns. Therefore, multiple detection events per pulse were unlikely. The maximum voltage from the readout SQUID (V_{SQ}) was on the order of 10 μV, and a room-temperature amplifier with 60 dB voltage gain was used for measurements. A diagram of the measurement apparatus is shown in the supplementary information of [21].

Figures 3(a) and (b) show the voltage across the SQUID as a function of time while optical pulses are directed at the SPD at a fixed rate. In figure 3(a) the integration loop inductance is 330 pH, chosen to store 16 pulses (4 bits), while that of figure 3(b) is 5.3 nH, chosen to store 256 pulses (8 bits). Discrete steps are evident with each laser pulse in figure 3(a) as a fluxon enters the integration loop. These are identical fluxon pulses, but here the measured response is nonlinear because it is convoluted with the response of the readout SQUID. The readout SQUID response is shown in the inset of figure 3(b). The same discrete steps are present in the response of figure 3(b) but are not discernible as they are smaller than the noise, which in this case is due to line noise coupled from our cryostat compressor to our measurement electronics. The full readout scheme, described in section 5, would eliminate both the nonlinearity and the noise. Figures 3(c) and (d) show statistical analysis of the small and large DI loops, respectively. The data points are the SQUID voltage averaged over 1000 independently measured traces. Each trace was taken after the number of photonic pulses indicated on the x-axis. The error bars give the standard deviation calculated from the 1000 traces. After each trace was generated and recorded, the current in the integration loop was erased by driving current through a PdAu resistor, fabricated in close vicinity to the inductor in the DI loop, L_{int}. To reset the state of the DI loop, a 10 mA current was applied to the resistor, which heated the inductor, broke superconductivity, and purged the integrated current in the loop.

To make sure the photon counters are working in SPD-SFQ mode in figure 3, we drove the SPD with current pulses that exceeded the switching current instead of relying on optical pulses. In this way we could change the width of the input pulses. An SPD-SFQ converter should output only one SFQ pulse for each input pulse, regardless of the duration of the input pulse. Figure 4(a) shows the device response for the current pulse width varying from 100 ns to 6.4 μs, in steps of a factor of two (geometrically spaced, i.e. 100 ns, 200 ns, 400 ns, 800 ns, 1.6 μs, 3.2 μs, 6.4 μs). No significant change in the output of the device is observed. The inductor in the integration loop can hold only around 16 SFQ pulses before it saturates. Because it does not saturate at a lower number of pulses when driven with a larger pulse width, we conclude the device is operating in the SPD-SFQ regime. In figure 4(b) we increased the bias I_{b1} to the SFQ SQUID, from 80 μA to 90 μA, thus moving the circuit outside the SPD-SFQ regime. In this case the integration loop saturates with fewer pulses as we increase

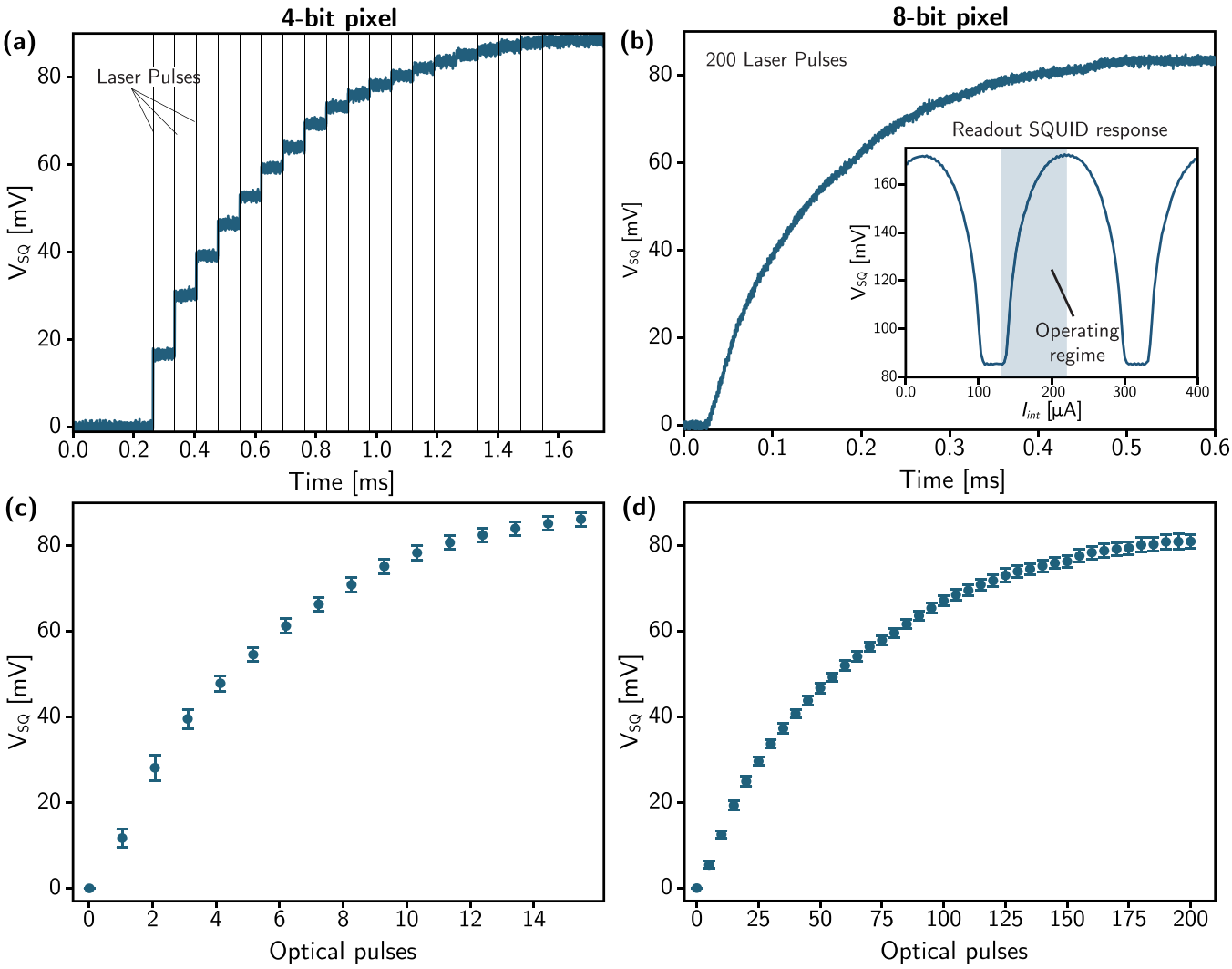

Figure 3. (a) Response of 4 bit pixel to a train of input optical pulses. (b) Response of 8 bit pixel. Inset shows the readout SQUID response curve. Shaded region shows the operating regime. (c) Statistical analysis of the pixel measured in (a). (d) Statistical analysis of the pixel measured in (b).

the pulse width. Furthermore, the readout SQUID voltage step should be less than $\approx 10\,\text{mV}$ for a single SFQ pulse, considering the inductance of the integration loop, room temperature amplification, and operating point on the readout SQUID response curve. Hence, at around 80 μA SFQ-SQUID bias, the device is working in the desired SPD-SFQ mode, while by 90 μA SFQ-SQUID bias it is no longer producing exactly one fluxon per photon detection event.

In addition to the digital SPD-SFQ operation just described, we have conducted measurements of similar circuits operated in analog, power-meter mode. For this demonstration, a slightly different circuit was used wherein the initial transduction SQUID (referred to as SPD-SFQ up to this point) had more symmetric inductances, compared to the counter ($L_1 = 9.2\,\text{pH}$ and $L_2 = 5.4\,\text{pH}$ in figure 1(a)). This more symmetric design is employed to implement the analog as opposed to digital transduction operation. The modified circuit also included a resistor in the integration loop, providing a leak rate. Thus, the circuit used in this part of the study is an analog power meter as opposed to the digital photon counter demonstrated in figure 3. In this mode, the initial transduction SQUID produces a stream of fluxons with each detection event. The number of fluxons generated with each detection event is determined by the bias current I_{b1}, which provides a control knob to adjust the response of the pixel based on the light level. The decay time here is around 6.25 μs, which is determined by the L/R decay time of the integration loop. For sufficiently long pulse trains at a given frequency, the device reaches a steady state that can be tuned with I_{b1}. Figure 5 shows the voltage on the readout SQUID as a function of the frequency of input photonic pulses. The different traces correspond to different values of I_{b1}, and this dynamically variable control parameter can be used to adjust the response to keep the pixel in a useful dynamic range. For a given value of I_{b1} and a given input rate of photons, the pixel will reach a different steady state value, which can then be used to

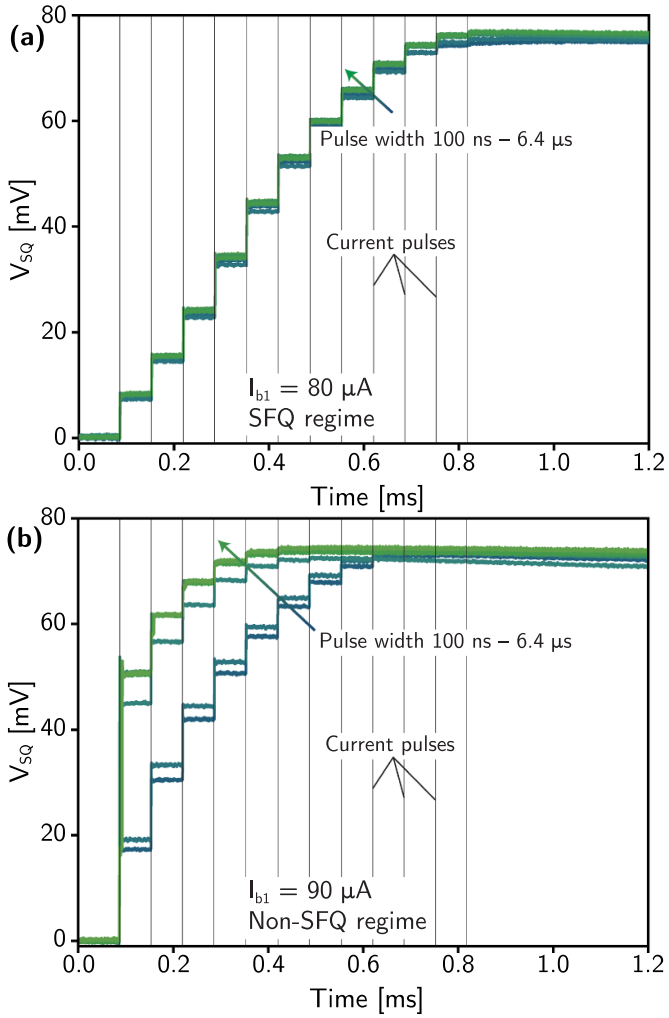

Figure 4. Photon counter response for different input pulse widths (i.e. 100 ns, 200 ns, 400 ns, 800 ns, 1.6 μs, 3.2 μs, 6.4 μs). The curves transition from dark blue to light green as the pulse width is increased. (a) The SQUID bias is 80 μA, which results in SFQ operation. (b) The SQUID bias is 90 μA, which is not in the SFQ regime. The slight decrease of current with time is due to a DC block filter.

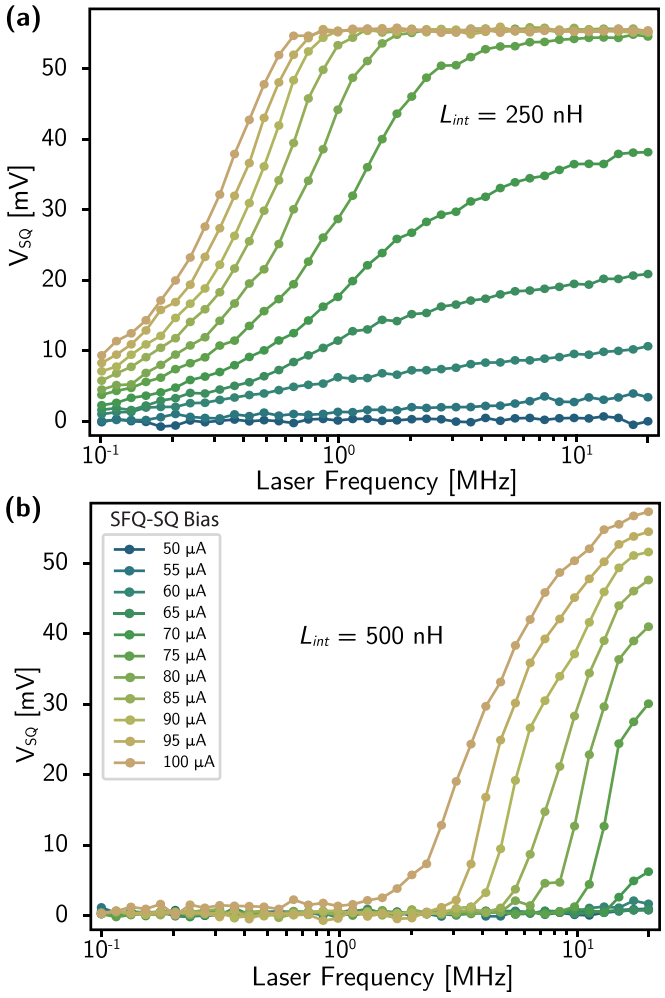

Figure 5. Steady-state SQUID voltage as a function of laser pulse frequency at different values of SFQ-SQUID bias, I_{b1}. (a) DI loop inductance is 250 nH. (b) DI loop inductance is 500 nH.

determine the incident light flux through a calibration procedure. Figure 5 shows the measured SQUID voltage as a function of the incident pulse rate for values of the bias current I_{b1} from 50 μA to 100 μA, demonstrating tuning across several orders of magnitude in incident photon flux. These are the transfer functions that can be used to determine the rate of incident photons. Figure 5(a) shows data for the device with 250 nH inductance in the DI loop, while figure 5(b) has an inductance of 500 nH. We see that with this range of input signal rates and integration-loop leak rate, the dynamic range of the smaller capacity loop is better matched to the signal.

During our experimentation we discovered that reading SPD pulses through Josephson electronics can reduce the effect of amplifier noise compared to standalone SPD readout. In the standalone SPD readout scheme, the SPD is connected to an amplifier through a bias tee. If there are high frequency reflections from the amplifier, they will pass though the bias tee and affect the SPD. This amplifier noise will result in lowering the SPD operating range and limit the device operation to a smaller plateau. On the other hand, in the integrated SPD scheme reported here, the SPD is not connected to a bias tee. It is well isolated from the amplifier though two superconductor SQUID transformers, leading to a more stable SPD bias current. Figure 6 shows the count rate versus SPD bias current for both a standalone and an integrated SPD that were fabricated on the same wafer, with the same geometry, and located in close proximity on the chip. For the integrated SPD we used the power-meter device with a leak in the integration loop. For sufficiently low laser frequency, the decay time in the DI loop is smaller than the separation of laser pulses. Therefore, individual voltage pulses were discernable and could be counted using a commercial pulse counter. We used a laser pulse frequency of 50 kHz for both the standalone and integrated SPDs. In figure 6(a), the room temperature amplifier used has a lower cutoff frequency of 50 MHz, and therefore frequencies below

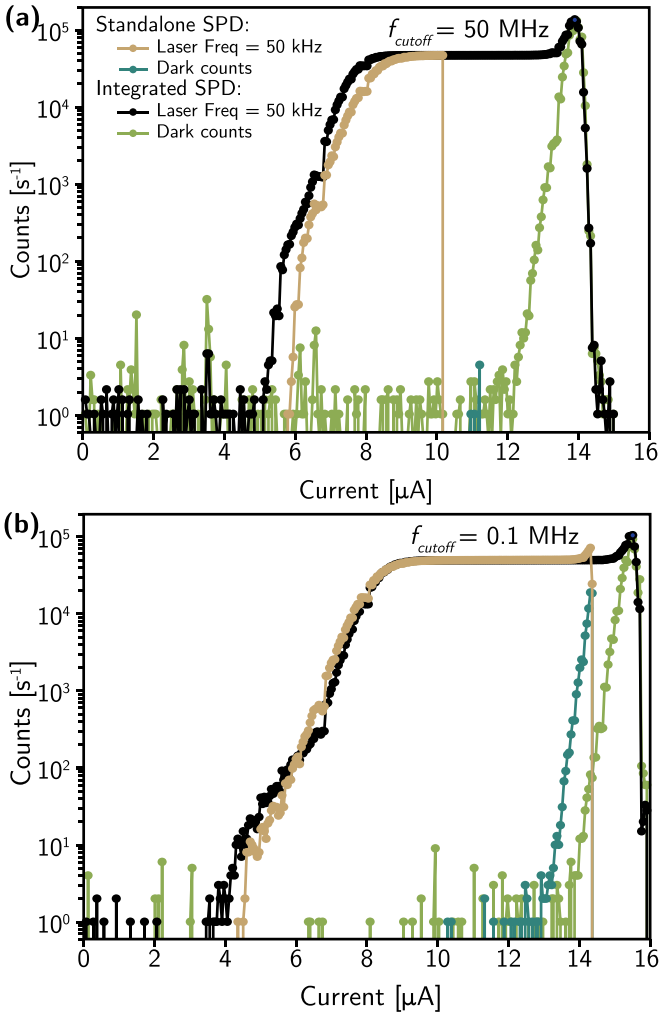

Figure 6. Comparison of readout performance from a standalone and integrated SPD with a 780 nm wavelength laser. (a) Using a room temperature amplifier with a 50 MHZ lower cutoff frequency and (b) using a room temperature amplifier with a 0.1 MHZ lower cutoff frequency.

50 MHz are expected to reflect from the amplifier. This lowers the operating range of the standalone SPD. On the other hand, the integrated SPD is not affected by the reflection, resulting in a factor of three improvement in the width of the plateau region. Figure 6(b) shows the same experiment but with an amplifier of 0.1 MHz lower cutoff frequency. Here the plateau region of the standalone SPD comes closer to matching that of the integrated device, yet the integrated SPD still has a larger plateau region by roughly 15%. Regarding dark counts, as seen in figure 6, the dark count rate is four orders of magnitude lower than the input pulse rate and had a negligible impact on the measurement.

Throughout this work we did not observe any effects of the light on other parts of the circuit aside from the SPDs. Most wiring is formed from 200 nm thick Nb, which shows no response to optical illumination at the levels used here. Some large inductors are formed from the same MoSi film as the SPDs, but these inductor meanders were much wider than the SPDs (4 μm as opposed to 200 nm) and were covered by a block of an upper Nb layer.

5. Summary and discussion

We have proposed and demonstrated a single-photon-counting pixel that functionally resembles a CMOS sensor pixel. The concept is made possible by the monolithic integration of SPDs with JJs. We have shown here that such pixels can store the signals from several hundred photon-detection events as supercurrent for later readout. This transduction of photons to stored supercurrent relies on the interface between SPDs with DC-SFQ converters. We have shown that the same basic circuit concept can be used to form a leaky integrator pixel that retains information about the average photon flux incident within a time period set by the leak rate of the integration loop.

In all modes of operation, the signal of interest is supercurrent in an inductor. To achieve scalability matching that of CMOS sensor arrays, it is necessary to extend the work here to include a readout architecture that will allow the interrogation of these supercurrents stored in arrays of millions of pixels. While multiple approaches to this technical challenge may be possible, we contend that further integration of SPDs and JJs with CMOS readout electronics offers a uniquely scalable approach to the problem. The integrated current in each pixel can be read out with transistors in an architecture very similar to that of CMOS sensor arrays. To interface superconducting electronics to semiconducting electronics, superconducting signals must be stepped up in voltage. Recent work on superconducting thin film amplifiers has significantly improved semiconductor–superconductor interfaces [29, 30]. In the superconducting state these amplifiers have zero resistance and can carry appreciable currents. When switched to the normal state by a current pulse, they transition to a high resistance state within less than a nanosecond, producing the voltage required to switch a MOSFET. These superconducting amplifiers are referred to as hTrons, and the circuit diagram of figure 7 shows an hTron interfacing the integration portion of the pixel to the CMOS readout circuitry. After an integration period, the DI loop contains a current proportional to the number of photons that have been detected. At read time, MOSFET $M1$ provides a ramp that adds to the current through the hTron gate. When $M1$ begins its ramp, $M4$ begins delivering a fixed current to the integration capacitor, C_{int}. When the sum of the integrated current signal and the applied measurement current from $M1$ reach the hTron gate threshold, a voltage will occur across the hTron channel, switching the gates of $M2$ and $M3$, which form an inverter. When this inverter switches, it cuts the voltage to $M4$, terminating the flow of current to C_{int}. After this operation, the charge on C_{int} is inversely proportional to the current that was present in the integration loop. This charge now serves as a proxy for the number of photons that were detected during integration. With the desired information represented as charge on a capacitor, the remainder of the readout follows a CMOS sensor array exactly. To read the charge on

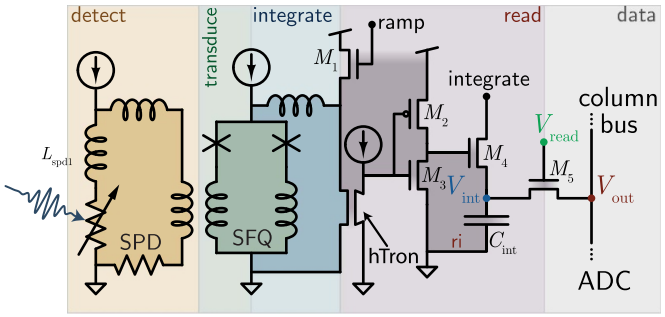

Figure 7. Circuit concept combining SPD, SQUID transduction, integration loop, and CMOS readout.

C_{int}, *M5* is opened, and the charge is coupled to the column read bus. When the hTron reaches its threshold, the current in the DI loop is erased, so the measurement of the state of the loop is destructive, and integration begins again with an empty loop.

Here we have shown the utility of integrating SPDs with JJs to increase the functionality of each SPD pixel. By further integrating these superconducting components with semiconductor electronics, significant further capabilities in array readout will be enabled. The full semiconductor-superconductor integration will be the subject of future work.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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